WHAT IS CLAIMED IS:

1. An asynchronous transport stream receiver of a digital broadcasting receiving system comprising:

a FIFO section for storing MPEG data generated based on a DVB-ASI (Digital Video Broadcasting Asynchronous Serial Interface) mode;

an oscillator for generating clock signals;

a controller for reading and outputting the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator.

2. The receiver according to claim 1, wherein the controller is operative to demultiply the clock signals of the oscillator by a predetermined times and is synchronized with the demultiplied clock signals.

3. The receiver according to claim 1, wherein the controller comprises a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator; a comparator for detecting sync byte; a counter for counting the MPEG data in terms of a packet unit of 188 bytes; and an MPEG data state decider for deciding a state of the MPEG data outputted from the FIFO section.

4. The receiver according to claim 3, wherein the MPEG data state decider outputs valid signals of the MPEG data if Ox47 byte detected by the comparator is the sync byte.

5. The receiver according to claim 5, wherein the counter is operative to check the MPEG data at least twice in terms of a packet unit of 188 bytes to ensure that the detected Ox47 byte is the sync byte.

6. The receiver according to claim 4, wherein the FIFO section generates a flag signal if the MPEG data stored therein is greater than a predetermined size.

7. The receiver according to claim 1, wherein the controller is an FPGA (Field Programmable Gate Array).

8. The receiver according to claim 1, wherein the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator is forwarded to an SD or HD leveled MPEG decoder for a subsequent processing.

9. A method for transmitting an asynchronous transport stream of a digital broadcasting receiving system having an FIFO section for storing MPEG data generated based on a DVB-ASI (Digital Video Broadcasting Asynchronous Serial Interface) mode and an oscillator for generating clock signals, the method comprising the steps of:

detecting whether the MPEG data is stored in the FIFO section;

if detected, retrieving the MPEG data from the FIFO section in synchronization with the clock signals of the oscillator;

detecting sync byte from the retrieved MPEG data; and

generating valid signals indicative of the MPEG data when the sync byte is detected.

10. The method according to claim 9, wherein the retrieving step includes demultplying the clock signals of the oscillator by a predetermined times and reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals.

11. The method according to claim 10, wherein the detecting step of sync byte sets the FIFO section into a read state.

12. The method according to claim 10, wherein the detecting step of sync byte comprises the sub-steps of:

detecting Ox47 byte from the MPEG data, and

checking whether the Ox47 byte is sync byte using a counter.